## REMARKS

The application has been carefully reviewed in light of the Office Action dated September 26, 2003. Claims 14, 15 and 16 have been cancelled without prejudice. Claims 1-13, 17 and 18 are now pending in this case.

Claim 1 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants respectfully traverse the rejection and request reconsideration. The Office Action states that the limitation "sensor[[s]]" does not have sufficient antecedent basis. Applicants respectfully submit that this limitation is correctly read as "said image sensor substrate," for which there is sufficient antecedent basis. That is, the word "sensors" was merely amended in the paper filed July 25, 2003 to be "sensor." Under PTO amendment drafting rules, it is proper format to use double brackets ("[[ ]]") instead of strikeouts to signify the canceling of the letter "s" at the end of the word, thereby making it a singular "sensor." Accordingly, claim 1 is in full compliance with § 112.

Claims 1-12, 14, 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Spivey et al. (U.S. Patent No. 5,886,253), in view of Sayag et al. (U.S. Patent No. 5,510,623), in further view of Thevenin et al. (U.S. Patent No. 5,937,027), and still further in view of Heller et al. (U.S. Patent No. 6,396,539), and still further in view of what is called "Applicants admitted prior art." Applicants respectfully traverse the rejection and request reconsideration.

Applicants respectfully submit that the Office Action, through its tenuous reasoning in attempting to string together four different references, in addition to what is

referred to as Applicants' admitted prior art (a total of five separate and diverse references), while making several unfounded, yet strategically placed, presumptions in the process, has failed to establish a prima facie case of obviousness.

MPEP §§ 2142, 2143 provide guidance on the subject. According to § 2142, "the examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness." Section 2142 also states that in view of all the factual information, "the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious."

This section also states that knowledge of Applicant's disclosure must be put aside in reaching this determination and acknowledges that the tendency to resort to "hindsight" based upon Applicant's disclosure is often difficult to avoid. However, this section cautions that impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art. See MPEP § 2142.

MPEP § 2143 also delineates the three criteria for establishing a prima facie case of obviousness as : 1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; 2) there must be a reasonable expectation of success; and 3) the prior art reference (or references when combined) must teach or suggest all the claim limitations. As described below in greater detail, the Office Action has failed make a prima facie case of obviousness under the MPEP.

Claim 1 recites a CMOS image sensor circuit comprising "a first CMOS image sensor substrate having an image sensor portion" where the image sensor portion has "a first portion and a second portion." Claim 1 also recites that the image sensor substrate has "a first set of parallel edges including a first edge and a second edge," and "a second set of parallel edges different than said first set of parallel edges" including "a third edge and a fourth edge."

Claim 1 also recites that the image sensor substrate "extend[s] between said first edge, said second edge, and said third edge." Claim 1 further recites that row logic be "physically located inside the image sensor in place of a plurality of pixels." Claim 1 also recites that a pixel interpolator and chip driver circuitry are "located between said first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate."

While the Office Action acknowledges that Spivey does not disclose that the row logic be in place of a plurality of pixels, it points to Thevenin for such support. Thevenin, however, as described in the Office Action, discloses an invention for minimizing an object's exposure to x-rays. Almost incredibly, the Office Action then seems to sum up by stating that "it would have been obvious to . . . have used exposure monitoring in the x-ray imager of Spivey in order to optimize" (and the sentence ends here). Applicants submit that this illogical jump from x-rays to the present invention of a CMOS image sensor circuit cannot be used to support a rejection under § 103.

Further, while the Office Action acknowledges that Spivey does not disclose a pixel interpolator between the first and second portions of the image sensor portion, it points to Sayag for this. However, as stated in the Office Action, Sayag discloses a centrally disposed read out register that is photosensitive in order to monitor exposure, thus, seemingly obviating the need for an interpolator. Yet, here too, the Office Action seems to sum up in stating that it would have been obvious to have had a centrally disposed photosensitive readout register (which is not even a limitation of claim 1) so as to monitor x-ray exposure in order to maximize image quality while minimizing radiation dose.

Here again, Applicants are at a loss as to what is so obvious with regard to the claimed invention since there is no claim limitation recited in this summation. In fact, the Office Action is seemingly applying non-analogous art in its five-reference "obviousness" rejection.

The Office Action later points to Heller as disclosing on-chip interpolation; however, rather than directly addressing the fact that Heller does not disclose the location of the interpolator as defined by claim 1, the Office Action improperly concludes that it would have been obvious to place the pixel interpolator between the image area and the fourth edge so as to enable butting and the creation of a large format array as taught by Spivey. Spivey, however, discloses a four-side buttable array. The four-side buttable array is not achievable using the structure defined by claim 1. That is, claim 1 defines a three-side buttable array. Accordingly, there is nothing so obvious about applying Spivey and Heller and arriving at this claimed invention.

Claim 2 depends from claim 1 and further recites that the row logic is formed in place of two columns of the array. Claim 2 is allowable over the cited references at least for the reasons mentioned above and also because none of the cited references, either alone or in combination, teach or suggest the invention defined by claim 2.

Claim 3 depends from claim 1 and further recites that the image sensor extends to within two pixel pitches of the first, second and third edges of the chip. The Office Action points to Spivey and although it acknowledges that Spivey does not disclose the limitations of claim 3, it states that it would have been obvious to make the edges on Spivey's image sensor to come within 2 pixel pitches instead of 4.

The Office Action seems to ignore the fact that Spivey discloses a row select shift register 186 which is itself at least 2-pixels wide and runs along only one edge of the chip. That is, the Spivey image sensor cannot extend to within two pixel pitches for each of the first, second and third edges of the chip, nor would it be obvious to do so for only the three sides of the chip as defined by claim 3.

Claims 4-7 depend from claim 1 and are allowable at least for the reasons mentioned above and also because none of the references, taken alone or in combination, teach or suggest the respective inventive combinations defined by claims 4-7.

Claim 8 recites a method of operating a large format image sensor comprising obtaining an image sensor chip "including row selecting logic in place of a plurality of central pixels of the image sensor," and "abutting [the] image sensor chip against a similar image sensor chip of corresponding construction." Claim 8 also recites "interpolating

missing pixels caused by both [the] row select logic and by spaces between [the] image sensor chips."

The Office Action states that the same reasons for rejecting claims 1 and 3 also apply to claim 8. Applicants respectfully traverse the rejection and request reconsideration. Nowhere do any of the references, either individually, or when combined, teach or suggest that interpolation be conducted on missing pixels caused by both row select logic and spaces between image sensor chips.

Claims 9, 11 and 17 respectively recite a CMOS imager and methods for fabricating the same as well as limitations similar to those of claim 1 and other limitations. Accordingly, the same reasons for the allowability of claim 1, as mentioned above, also apply to claims 9, 11 and 17.

Claim 10 depends from claim 9 and is allowable at least for the same reasons as claim 9 and also because none of the references, taken alone or in combination, teach or suggest the inventive combination defined by claim 10.

Claim 12 depends from claim 11 and is allowable at least for the same reasons as claim 11 and also because none of the references, taken alone or in combination, teach or suggest the inventive combination defined by claim 12.

Claim 14 has been cancelled without prejudice and therefore the rejection is no longer applicable.

Claim 18 depends from claim 17 and is allowable at least for the same reasons as claim 17 and also because none of the references, taken alone or in combination, teach or suggest the inventive combination defined by claim 18.

Claims 13, 15 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Spivey in view of Sayag and further in view of Thevenin. Applicants respectfully traverse the rejection and request reconsideration.

Claims 15 and 16 have been cancelled without prejudice and, therefore, the rejection as to those claims is no longer applicable.

Claim 13 recites a CMOS image sensor circuit and also recites limitations similar to that of claim 1 and other limitations. Therefore, at least for the reasons mentioned above in connection with claim 1, claim 13 is also allowable.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue.

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Respectfully submitted,

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